ELECTRONIC BOARDS FOR SPATIAL APPLICATIONS

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ABSTRACT

A thermal model to predict the temperature distribution on the electronic boards of Argentinian satellite SAC-C is presented. A simple model of the box that contains the boards provides the boundary conditions for the thermal calculation of the boards itself. The 3D thermal problem of each board was solved with a novel 2D multilayer FEM developed by the authors. This approach is aplicable because no convection colling is present and thermal radiation can be conservatively neglected.

INTRODUCTION

Thermal management of electronic boards in satellites can be a problem if no special care is taken. Proper cold surfaces and conduction layers must be provided for the board and its components to release the heat towards the cold points in the satellite. As no transport fluid is present in open space, this cooling can be done by conduction and radiation only.

The present work outlines an approach for solving heat problems in electronic boards for spatial applications. The work was motivated by, and applied to, the thermal evaluation of the electronics boards of the Argentinian satellite SAC-C [1]. The present approach has been revised and aproved by NASA.

The aim is to properly estimate the maximum junction temperatures in the chips of the boards. These boards are attached to aluminum boxes through mounting bars that act as heat sinks. When compared to conduction through the board, the contribution of radiation to the cooling of the equipment can be neglected in this case. This is, furthermore, a conservative assumption. An estimate of the temperature of the base and top of the aluminium boxes, based on a balance of the total heat generated by the boards and the cooling provided by radiation from the box into the space, are used as boundary conditions for the electronic boards.

A novel multilayer variation of a standard 2D FEM solver for heat conduction problem is developed for solving the temperature field in the boards and the chips themselves. The solver is the heart of a set of utilities devised to allow for the calculation of a large number of different boards in a short time. In the next sections, a brief description of the method and the overall solution procedure is given. Some representative results obtained are also presented.

THERMAL MODEL OF THE BOXES

The boards are mounted in aluminum boxes, 6 in total in SAC-C, which are in turn fixed to the frame of the satellite in a platform (see figure 1). The roof and floor of this boxes, consisting of thick aluminium plates, can be considered isothermal bodies. Their temperatures are easily evaluated from the total thermal power generated by the boards of the box and the known temperature conditions of the platform (40 °C). Once defined, they serve as Dirichlet boundary conditions for the boards' thermal calculation.

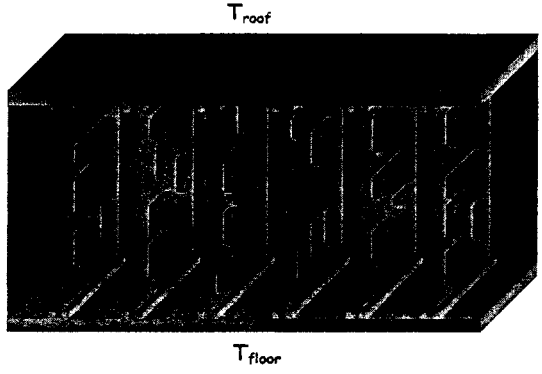

Figure 1: electronics box

MULTILAYER MODEL

The approach for solving the thermal problem in each board is based on the fact that the problem at hand, although 3D in nature, may be reasonably represent by 2D layers, parallel to each other, and thermally interconnected at some points, lines, or surfaces. The board itself, which we consider the base or lowermost layer, may be thought as a conducting plane due to the fact that the temperature gradients in the direction normal to this plane are negligible. On top of that layer, one or more additional layers are used to represent the integrated circuits, or chips. For our purposes, these chips may well be considered as conducting planes, due to the fact that the heat flows mainly through the connecting pins, which lay on a plane inside the casing of the chips.

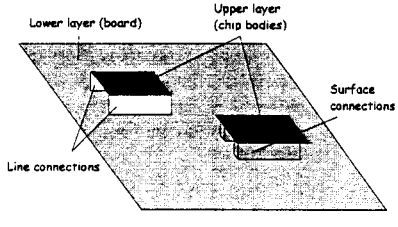

Figure 2: multilayer model of a board

The different layers are thermally connected with each other at the zones were chips or other components are attached to the board. The type of thermal connection depends on the chip's mounting procedure. For an isolated component, like a resistor, the thermal connections are just a set of points; for a typical chip with arrays of pins on one or more of its sides, the thermal connections can be thought of as a set of lines; and finally, for a typical high power component or dissipator, the mounting is done by sticking its base to the board with a heat conducting glue, so the thermal connection is best represented by a surface.

CHIPS DATABASE

Different types of chips and other components were identified, classified, and stored in a chip database. Some of the chips types identified are shown in Figure 3, along with a special component of arbitrary shape which we call conducting/generating zones, aimed at representing, for example, thermal dissipators.

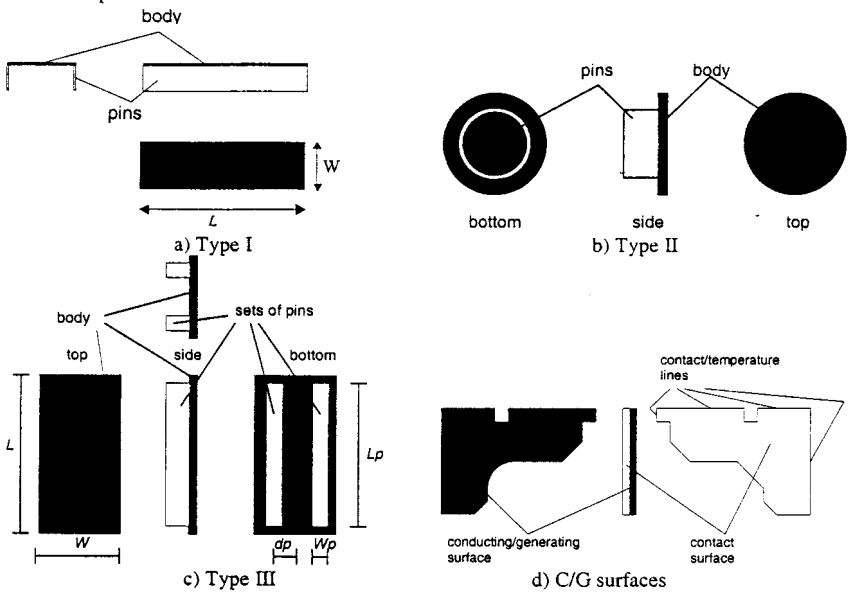

Figure 3: some types of chips and components

Each type has its own set of parameters that need to be assigned values in order for the component to be completely defined. For example, a chip of Type III requires the definition of all the dimensions shown in Figure 3-c, plus the power level and information about the equivalent conductivities of the body and the set of pins. The information contained in the database looks like the example tables below. Here, the symbols *h'*, *h"*, and *Tcj* stand respectively for the line conductivity coefficient of a row of pins, the surface conductivity coefficient of a 2D set of pins, and the maximum admisible junction temperature.

Type I Chips Name	*kb* [w/°C]	*L* [mm]	*W* [mm]	*h'* [w/mm°C]	*Tcj* [°C]
AD574AD	0.12	38.0	13.0	2.13x10-3	20.
HI-574A	0.12	38.0	13.0	2.13x10-3	15.
:	:	:	:	:	:
MC33035	0.12	16.0	10.0	2.13x10-3	15.0

:

Type III Chips Name	*kb* [w/°C]	*L* [mm]	*W* [mm]	*Lp* [mm]	*Wp* [mm]	*dp* [mm]	*h"* [w/mm²°C]	*Tcj* [°C]
BU-61582	0.14	48.2	25.4	44.9	4.3	6.3	0.04	7.2

:

etc.

NUMERICAL MODEL

The numerical approach is based on a modification (FEMINA [2]) of a standard 2D FEM thermal solver (MEFDIF [3]). The board and the electronic components were discretized by 2D Delaunay triangulations. The solver was modified to allow for the thermal connections between different layers. The connections were modeled, depending on its type, as Dirichlet conditions in internal nodes, mixed conditions on internal sides, or element sources. All of these conditions depend on nodal temperatures on some nodes of a different layer.

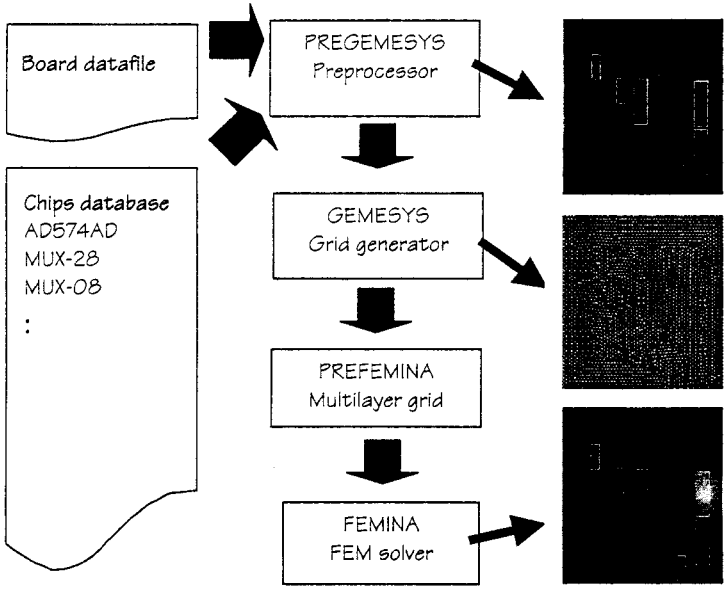

Figure 4: sketch of the solution process for each board

The whole calculation was automated to simplify the analysis of a large number of boards (see Fig. 4). First, a components database is prepared to hold the information of individual circuits (chips, dissipators, etc.). Second, a data file for each board is prepared, in which the only data needed is the location, orientation, and operating conditions of each chip, along with the geometry and thermal characteristics of the board (see Figure 5).

Third, an ad-hoc grid preprocessor, PREGEMESIS [4], reads the datafile for the specific board being analyzed, gathers information about the specific circuits being used from the components database, and builds an input file for the automatic grid generator GEMESIS [5].

The fourth step involves running the grid generator GEMESIS to create a single-layered grid. Next, an ad-hoc FEM preprocessor, PREFEMINA [6], reads the single layered grid provided by GEMESIS and creates the corresponding multilayered grid. The sixth step involves solving the resulting pseudo-3D thermal problem with FEMINA. Finally, the temperature fields are analyzed with the aid of the graphical postprocessor CONTOUR2D [7]. Examples of temperature fields obtained for some of the boards analyzed are shown in Figure 6.

```
*TITLE
```

```
        Board EL142
*COMPONENT                                  power  xcenter  ycenter  rot
        C=AD574AD       parameters           0.6,   135.,    76.5,   1
        C=MUX-28        parameters           0.2,    76.,    78.5,   1
        C=MUX-28        parameters           0.2,   135.,    35.5,   1
        C=MUX-08        parameters           0.2,    32.5,  108.,   1
        C=MUX-08        parameters           0.2,    56.5,   88.,   1
        C=MUX-08        parameters           0.2,   114.5,   14.,   1
*BOARDS
        B=GROUNDPLANE2
        parameters      0.7,
        keypoints       4,   0.,   0.,   156.,   0.,156.,  150.,   0.,  150.,
        line          1, 42.83,
        line          2,   0.,
        line          1, 46.61,
        line          2,   0.,
*END
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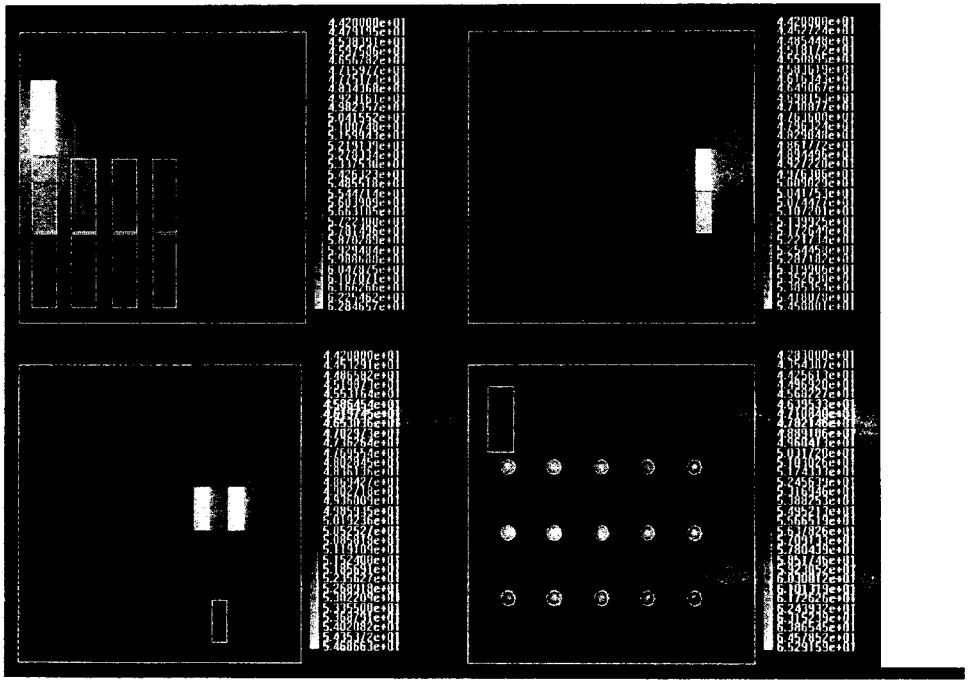
Figure 5: example of datafile for board EL142

Figure 6: some examples of temperature solutions



CONCLUSIONS

A novel 2D multilayer approach for dealing with 3D conduction problems in electronic boards for spatial applications has been presented. The key idea behind the method is the concept of layers of standard 2D FEM grids that connect to each other either at nodes, element sides, or element surfaces.

The package developed was used for the thermal evaluation of electronic boards of the Argentinian satellite SAC-C. Although in most of the boards the junction temperatures of the main chips were found not to exceed their design limits, some boards do revealed desing deficiencies. For those boards, design modifications were proposed and numerically tested before making the final recomendations. The results of this study were evaluated and approved by NASA itself.

Combined with a set of pre- and postprocessing utilities developed by other authors, the package developed using the proposed approach proved to be a fast and reliable way for analyzing tens of boards in just a few days of work. Although devised for a highly specific application, the idea of a multilayered 2D FEM may well find its way in other fields in the future.

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